REMARKS

Claims 1-7, 16-21 and 29-36 are all the claims pending in the application. Applicant amends claims 1, 2, 4, 17, 19, 33 and 34. The claim amendments are at least supported by FIG. 4 of the Applicant's disclosure. No new matter is added.

Statement of Substance of Interview

An interview was conducted between Examiner Tammy Pham and Applicant's representative Ebenesar D. Thomas on July 29, 2009. During the interview, Applicant's representative asserted that the combination of the cited references do not teach or suggest "wherein a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply", as recited in the independent claims. Further, Applicant's representative pointed out that these claimed features are at least described in paragraph 41 of the specification.

The Examiner acknowledged that paragraph 41 supports the claimed feature. Moreover, the Examiner suggested amending the feature of at least one signal line connected to each gate terminal of said first and second transistors in claims 1, 17, 33 and 34 to further define the claim. In addition, with regard to claim 2, the Examiner suggested amending the claim to recite that all the elements are on a single substrate.

Applicant has taken Examiner's remarks into consideration in preparing this Amendment under 37 C.F.R. § 1.111.

It is respectfully submitted that the instant Statement of Substance of Interview complies with the requirements of 37 C.F.R. §§ 1.2 and 1.133 and MPEP §713.04

Claim rejections under 35 U.S.C. § 112, second paragraph

The Examiner rejects claims 4 and 19 under 35 U.S.C. § 112, second paragraph for insufficient antecedent basis issue.

In view of the amendments to claims 4 and 19 submitted herewith, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. § 112, second paragraph rejection.

Claim rejection under 35 U.S.C. § 103

Claims 1-4, 6-7, 16-19, 21 and 29-36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No. 7,002,541) in view of Okajima (U.S. Patent No. 5,793,680).

Claims 5 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagi and Okajima and further in view of Park et al. (U.S. Patent No. 7,133,034).

Applicant traverses the rejection for at least the reasons agreed upon by the Examiner during the interview and following discussion below.

Claim 1

Claim 1, recites, *inter alia*, "at least one signal line connected to each gate terminal of said first and second transistors, which controls the switching of the first and second transistors."

In FIG. 5, Yanagi discloses an offset setting section 5 which includes resistances 5a and 5b, and a switch 5c. In each resistance 5a and 5b which functions as voltage setting means, the

d.c. standard potential Vref1 is applied to one end and the other end is grounded. However, Yanagi does not teach or suggest a signal line connected to each gate terminal of said first and second transistors, which controls the switching of the first and second transistors."

Furthermore, Okajima discloses a circuit diagram of a circuit which reverses the phase relation of the clock signal CLK supplied to internal elements depending on whether the latching operation starts at a rising edge or a falling edge. Applicant respectfully submits that it would not have been obvious to one of ordinary skill in the art at the time of the invention to replace the offset setting section which provides a d.c. standard potential Vref1 with the circuit of Okajima that reverses the phase relation of the clock signal. In particular, replacing a constant DC voltage at Vref1 with the output of the clock-pulse arrangement determination unit would change the primary function of the offset setting section of Yanagi. Therefore, one of ordinary skill in the art would not have been motivated to modify the system of Yanagi with the features of Okajima.

In addition, the combination of Yanagi and Okajima also fails to teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply."

Applicant submits that paragraph 41 of the specification describes that "according to this embodiment, a voltage difference between the gate and source of the PchTFT 41 and NchTFT 42 is larger compared to the voltages VCOMH and VCOML so that ON resistances of the PchTFT 41 and NchTFT 42 can be lowered." Accordingly, Applicant's specification does provide at least one advantage for the claimed feature discussed above according to an exemplary non-

limiting embodiment. At least for these reasons discussed above, Applicant submits that the voltage values of the signal lines are not an obvious matter of design choice.

Moreover, neither Yanagi nor Okajima teach or remotely suggest anything about the voltage levels of the signal passing through the signal line. Therefore, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have the high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and the low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply.

In view of the above, Applicant submits that claim 1 is patentable over the cited combination of the references.

Claims 17, 33 and 34

Applicant respectfully submits that claims 17, 33 and 34 recite subject matter analogous to claim 1, and therefore are allowable for at least analogous reasons claim 1 is allowable.

Claims 2-4, 6, 7, 18, 19, 21, 29-32, 35 and 36

Applicant submits that claims 2-4, 6, 7, 18, 19, 21, 29-32, 35 and 36 depend from one of the independent claims that have been shown to be allowable, and therefore these claims are allowable at least by virtue of there dependency and the additional features recited therein.

With regard to claim 2, Applicant respectfully submits that the cited combination of the references do not teach or suggest "at least said common drive circuit, a display portion and a gate driver circuit for controlling switching of pixels of each line in said display portion are mounted on a single substrate."

Claims 5 and 20

Applicant submits that since claims 5 and 20 depend from one of the claims that have been shown to be allowable and since Park does not teach or suggest the features of claim 1 missing in Yanagi and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

/Ebenesar D. Thomas/

Ebenesar D. Thomas
Registration No. 62,499

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860
WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: August 31, 2009